

AMENDMENT TO THE DRAWINGS

Please replace drawing sheets 3 of 12 through 12 of 12 (showing Figs. FIGS. 3, 4, 5A-5F, 6, 7A-7J, and 8) with the newly-submitted sheets attached herewith. Please note that in each of these figures, the numeral "0" showing the logic value for holding the state of TEST-LOGIC-RESET to loop back to itself has been changed to the numeral "1" in order to be consistent with the specification on p. 5, lines 3-5.

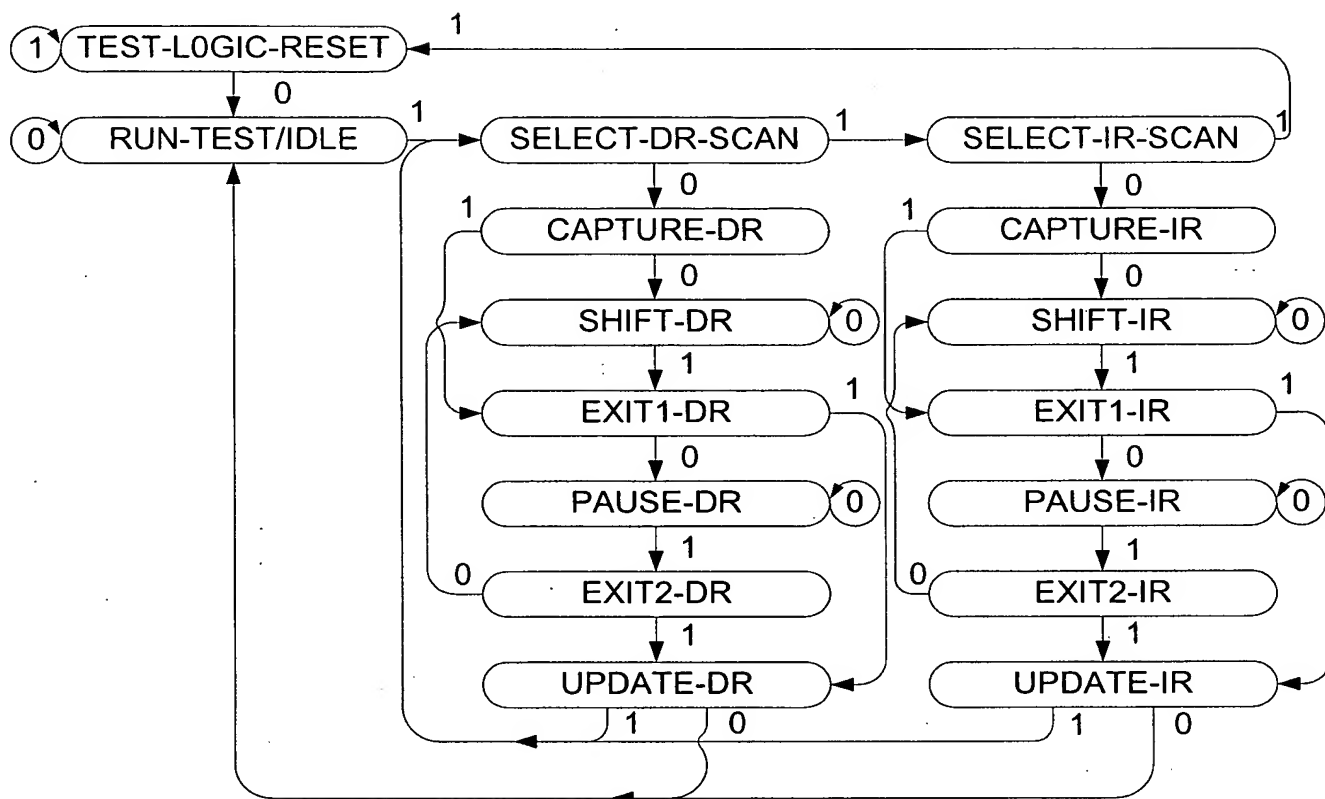


FIG. 3
(PRIOR ART)

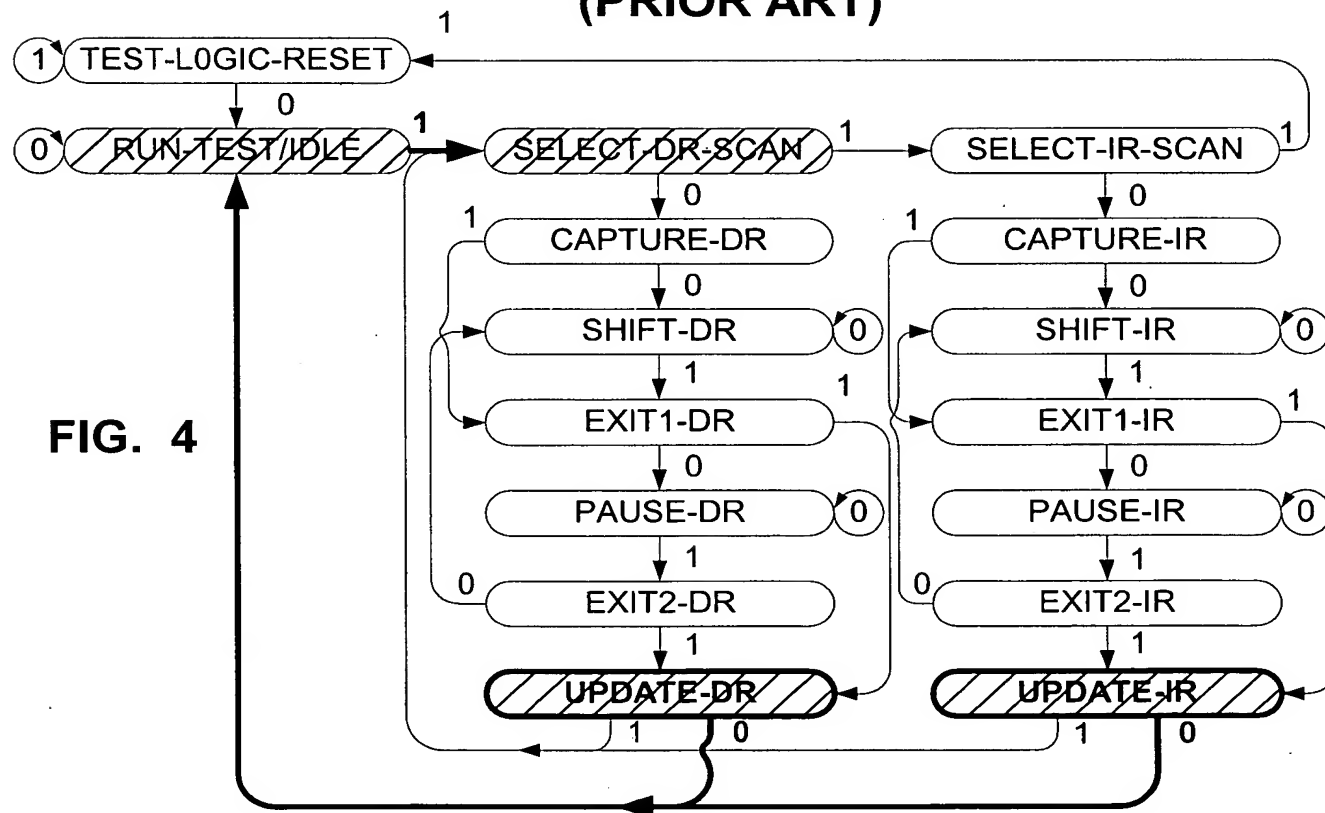


FIG. 4



FIG. 5A

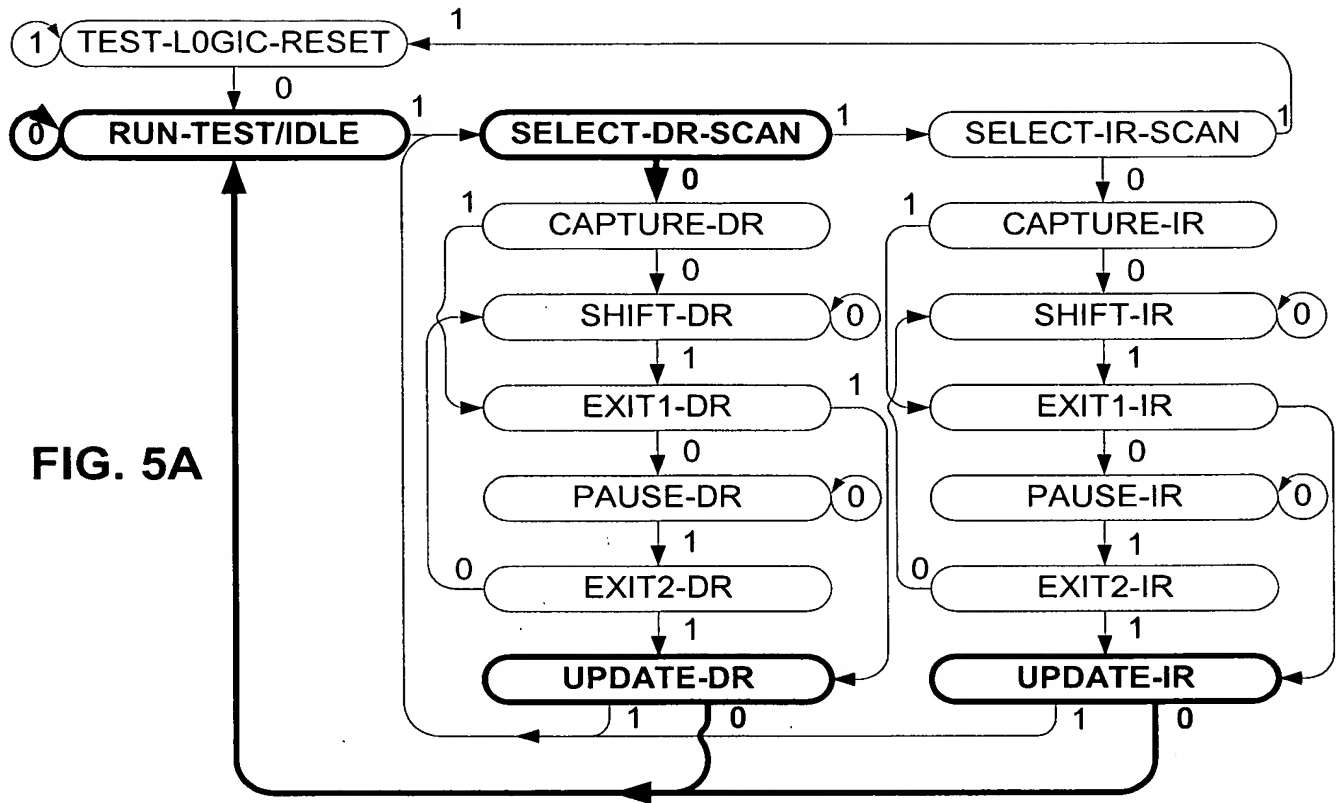


FIG. 5B

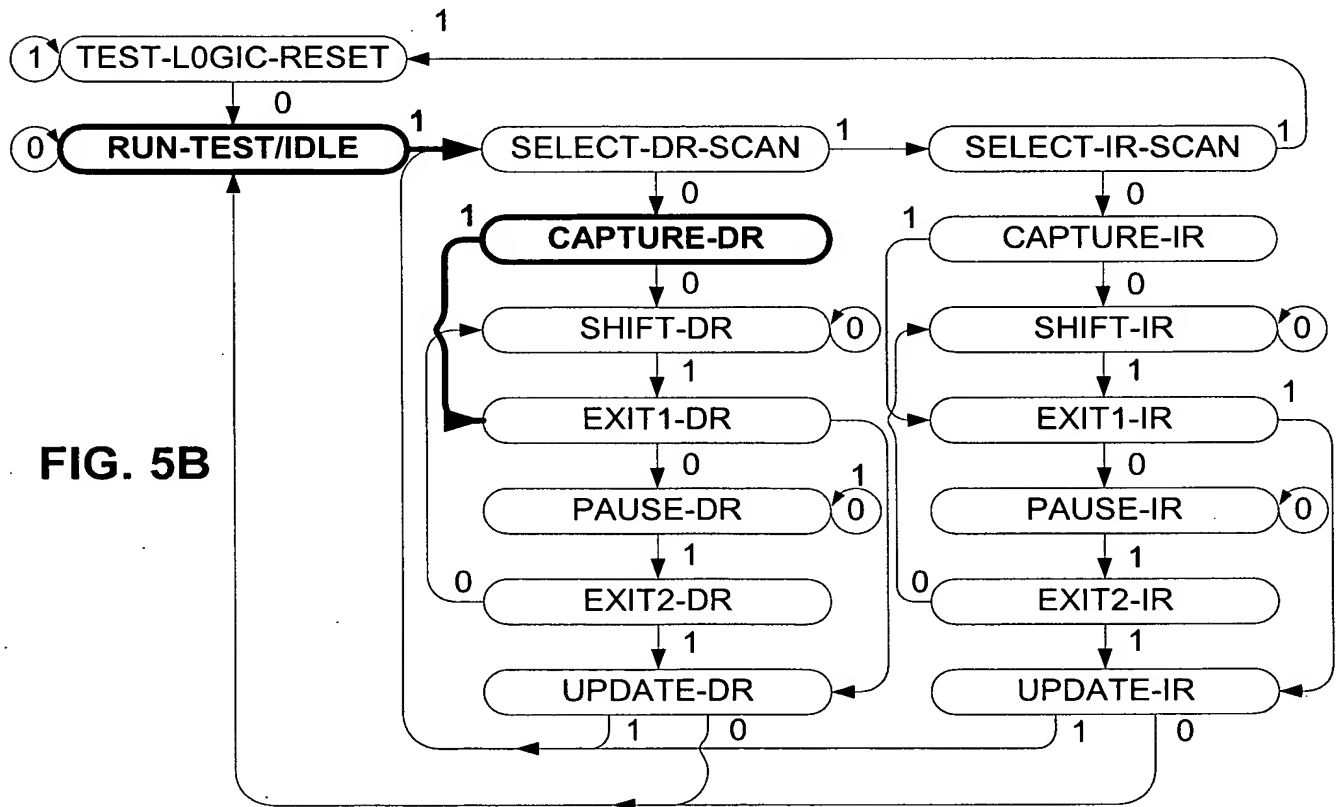




FIG. 5C

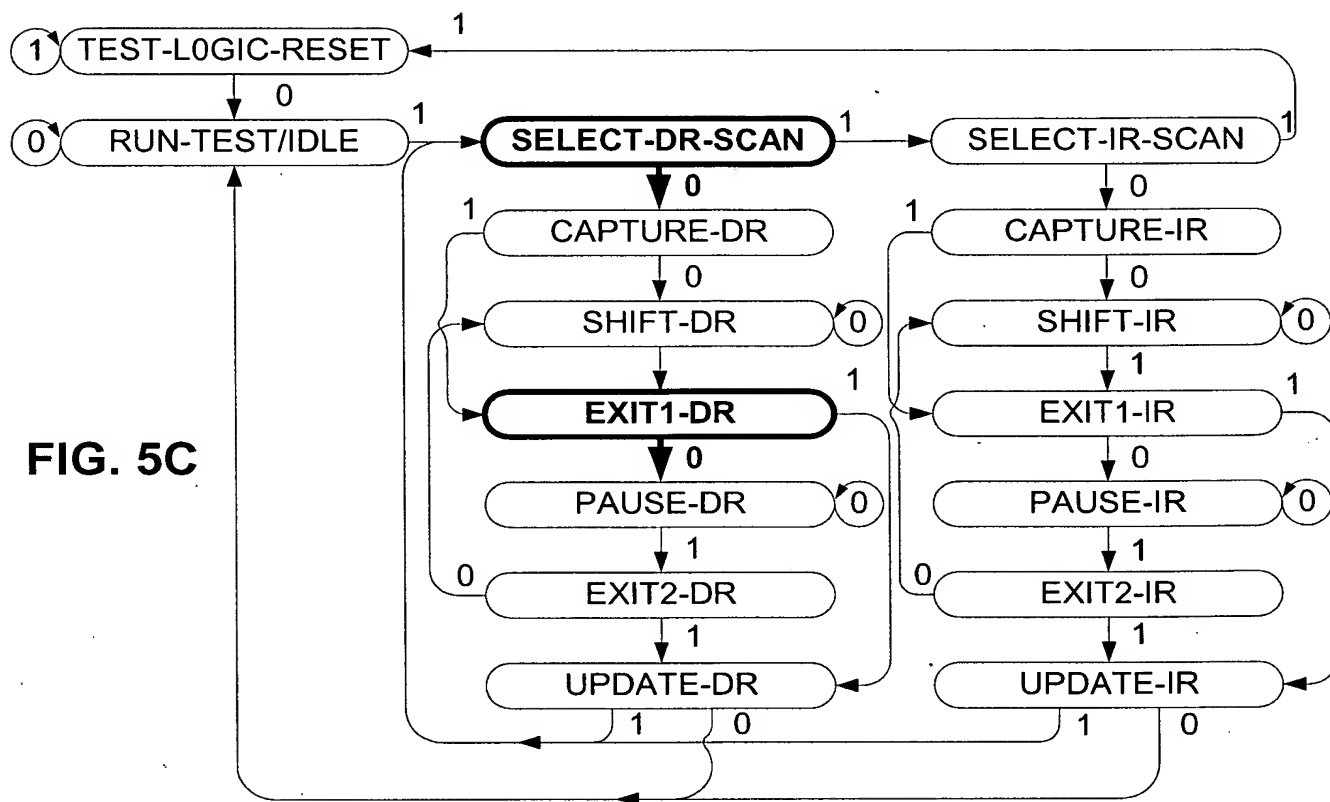


FIG. 5D

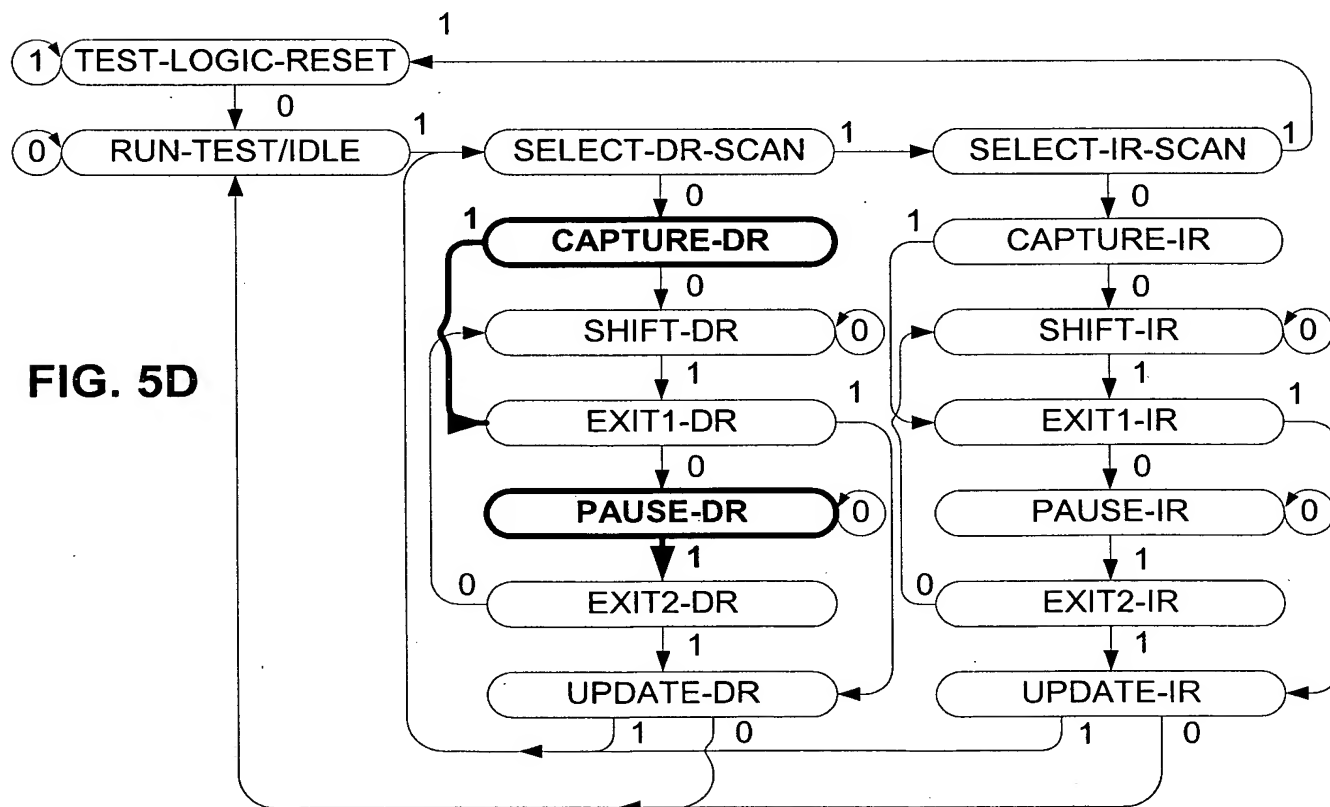




FIG. 5E

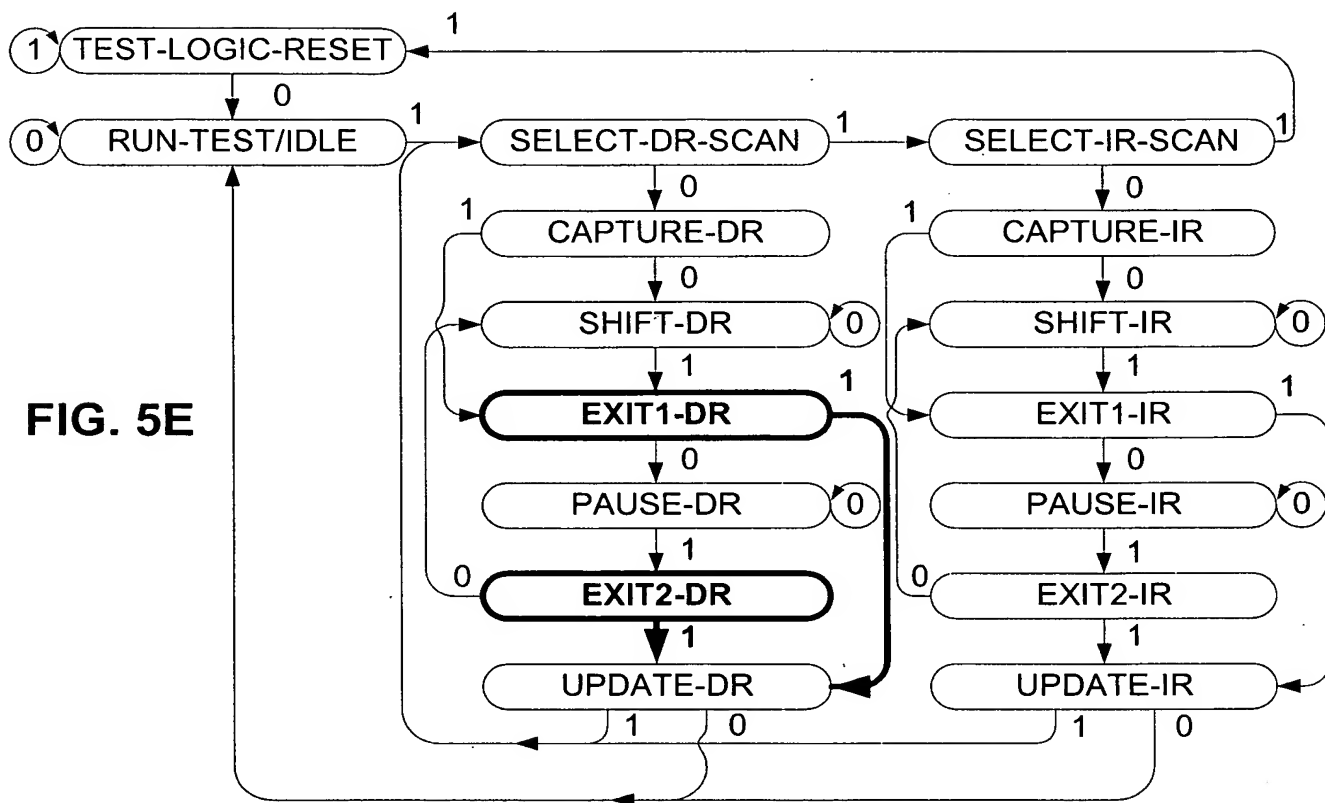
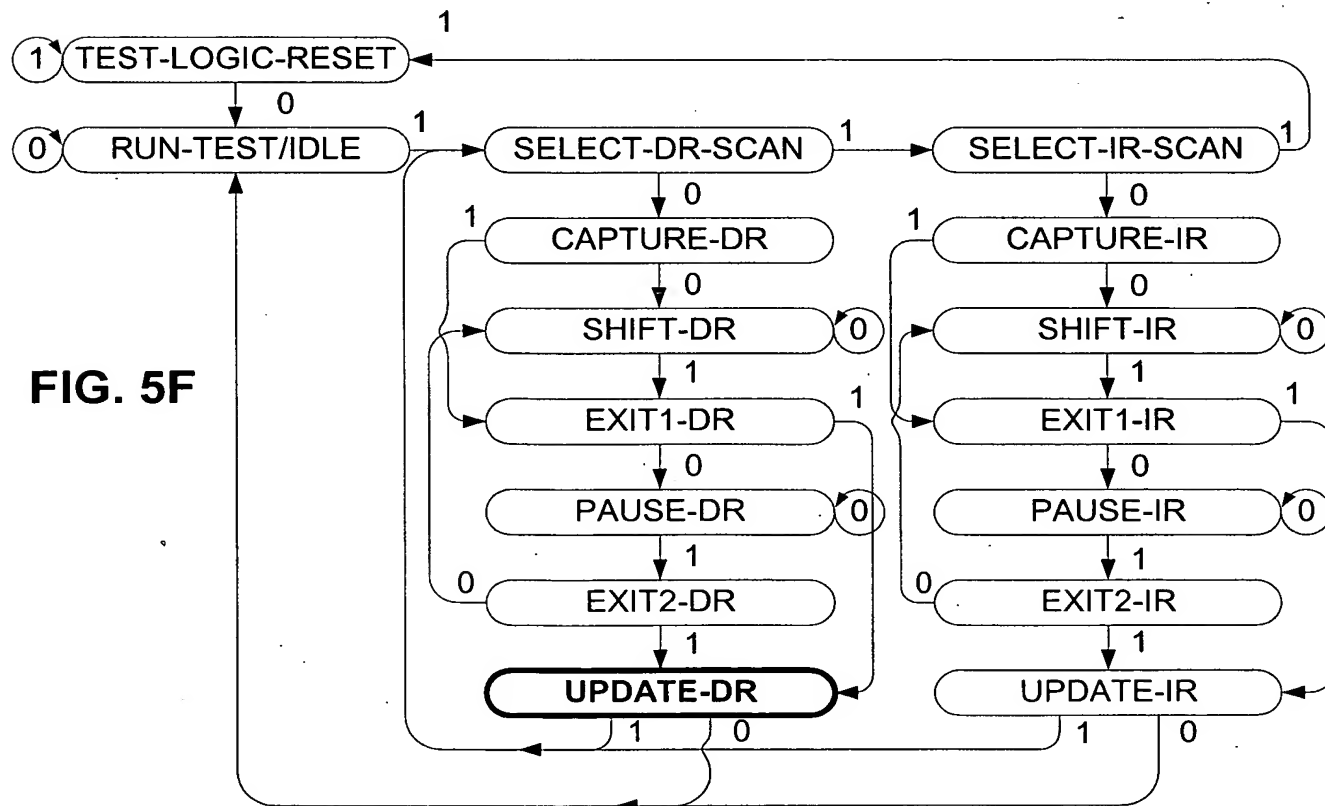
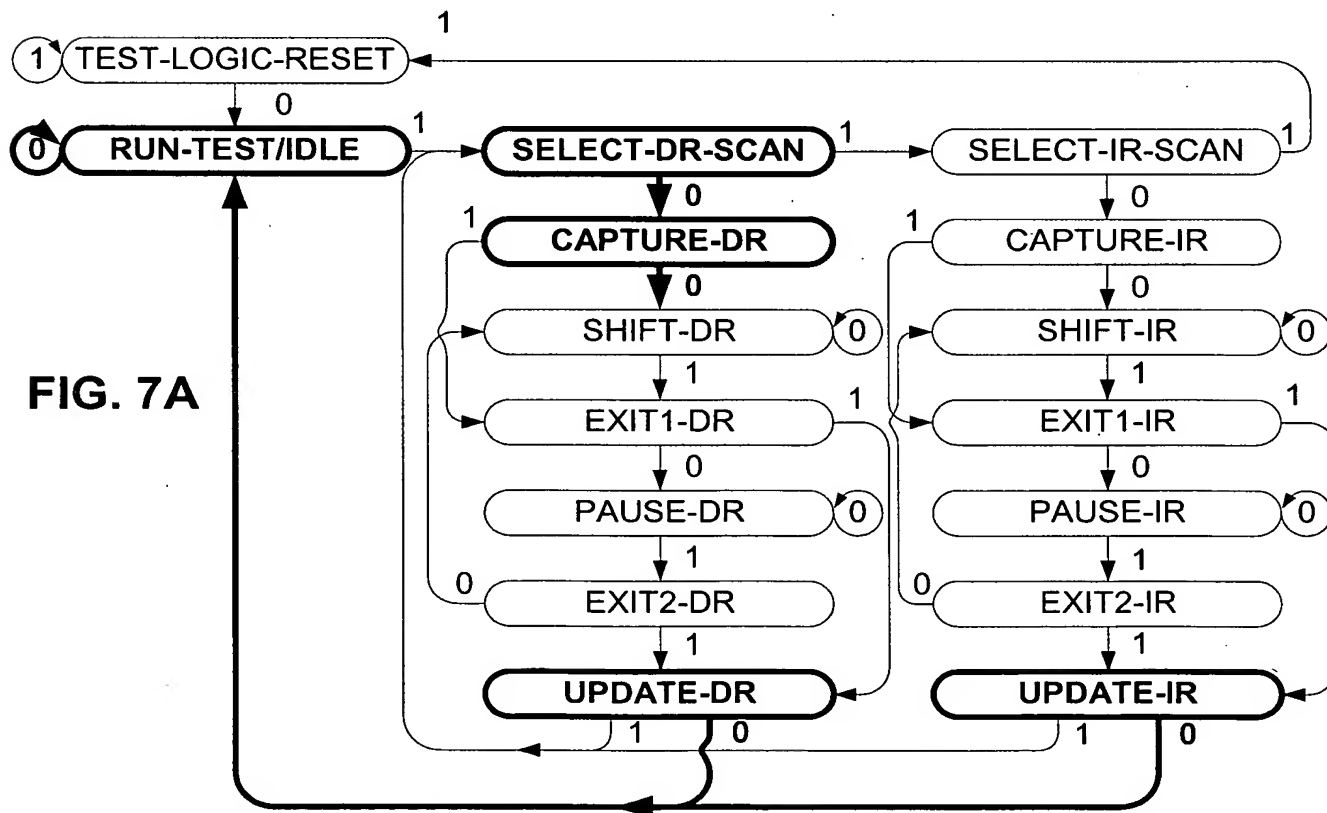
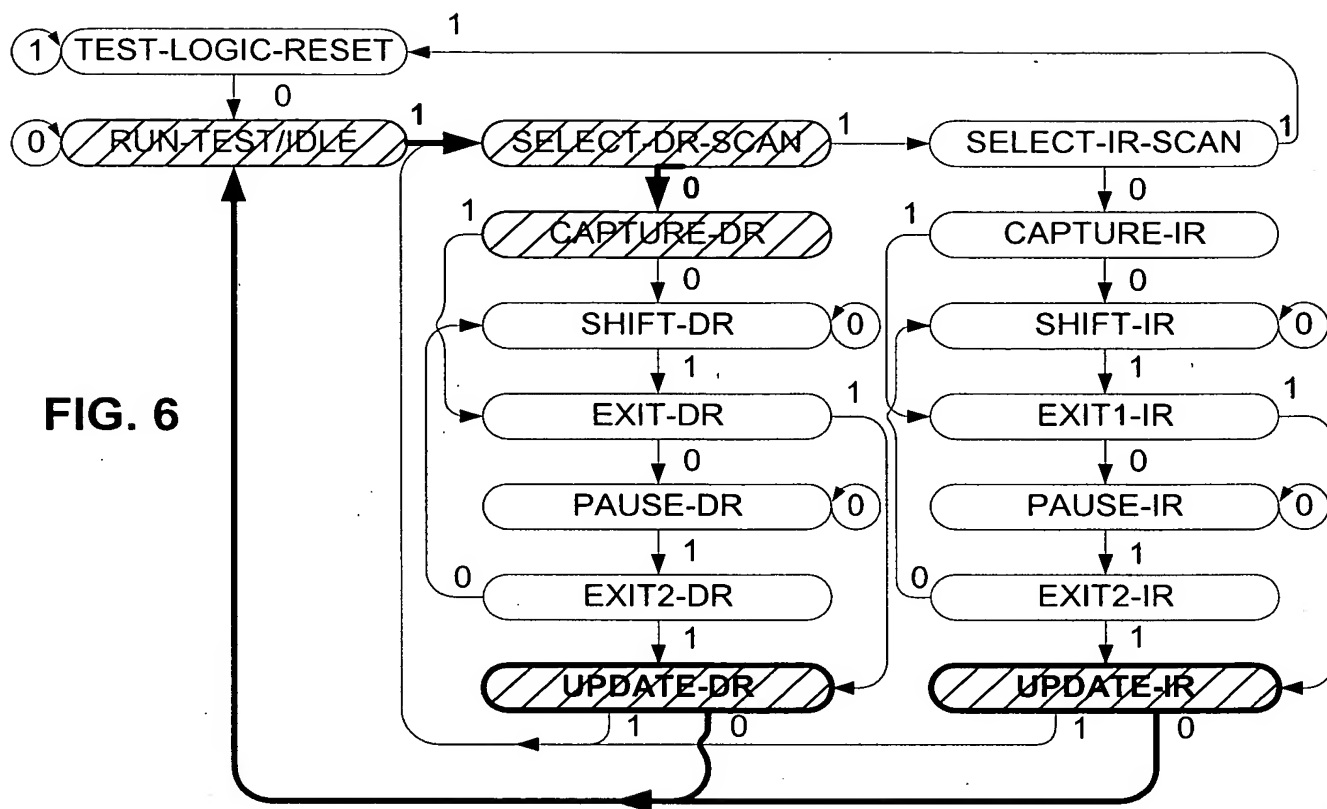


FIG. 5F





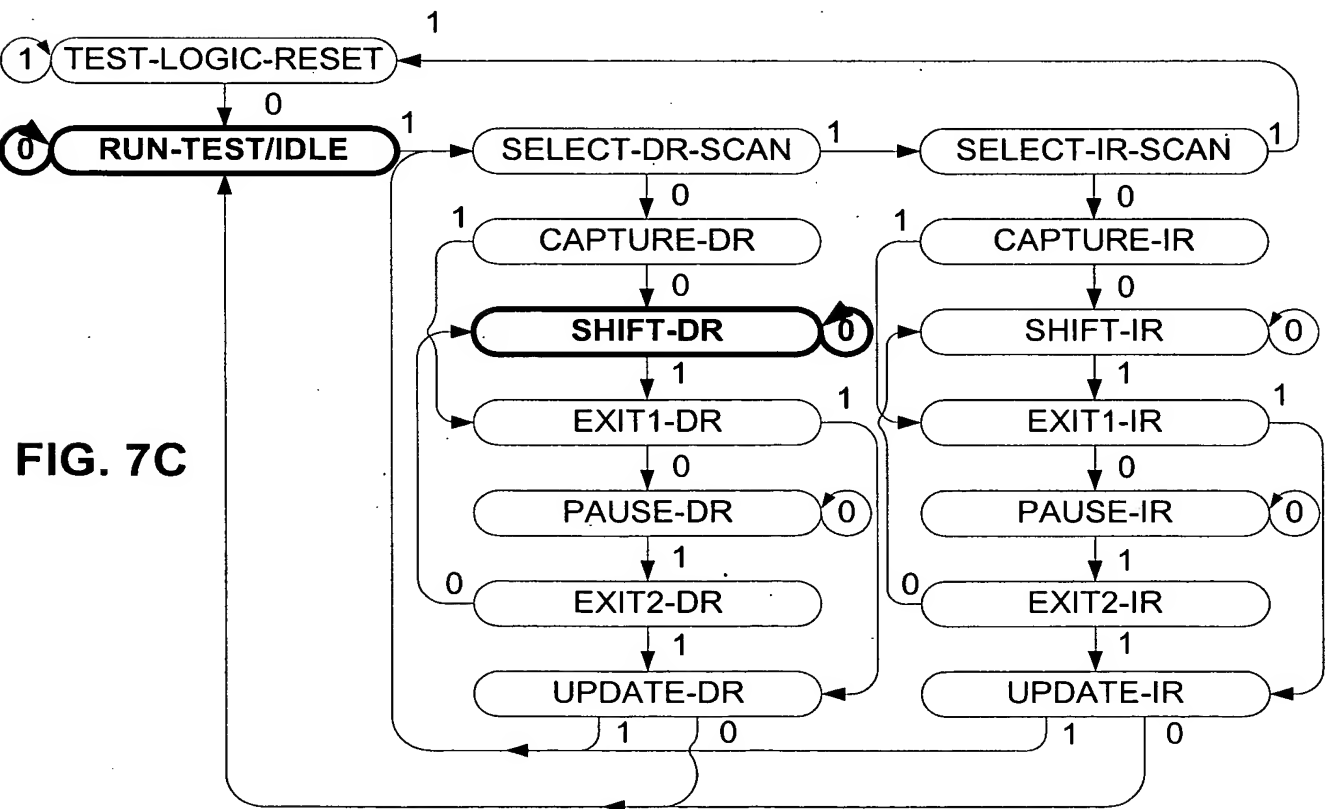
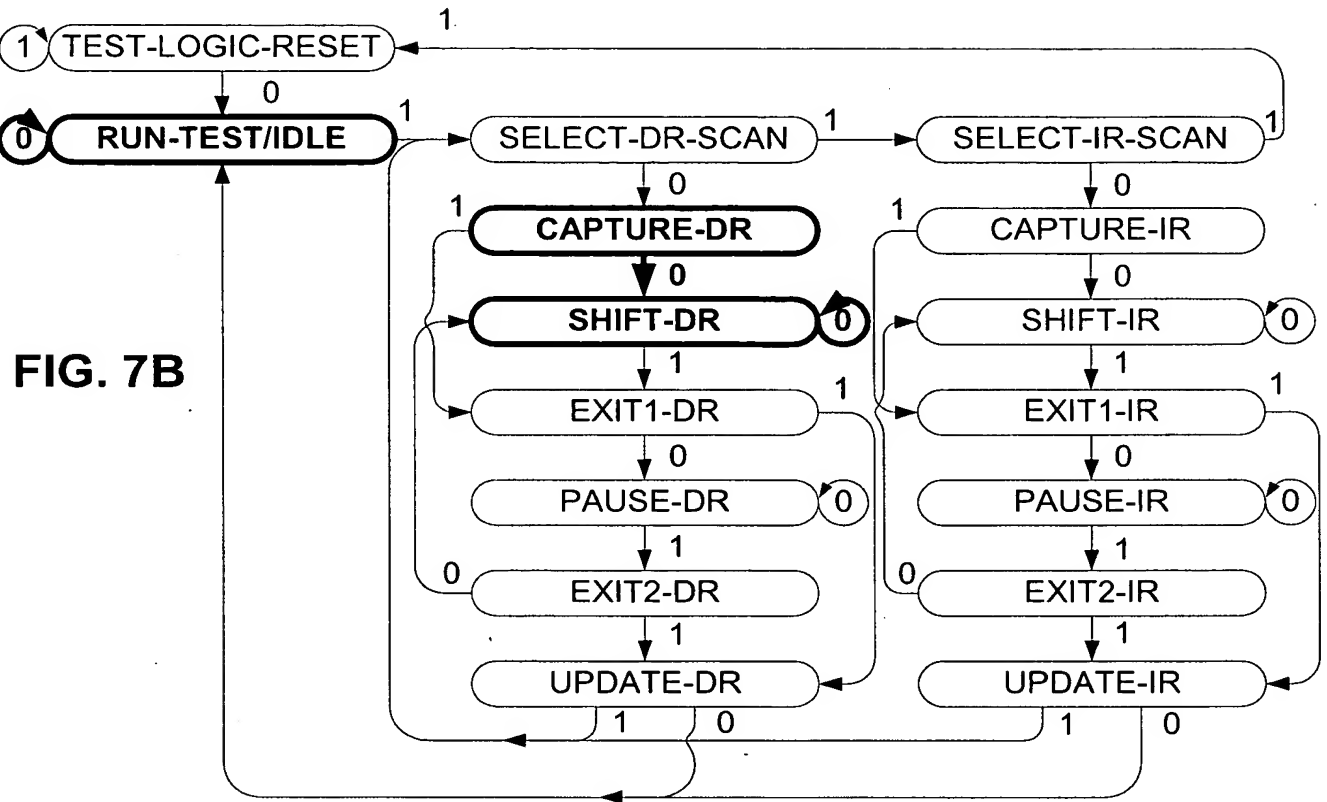




FIG. 7D

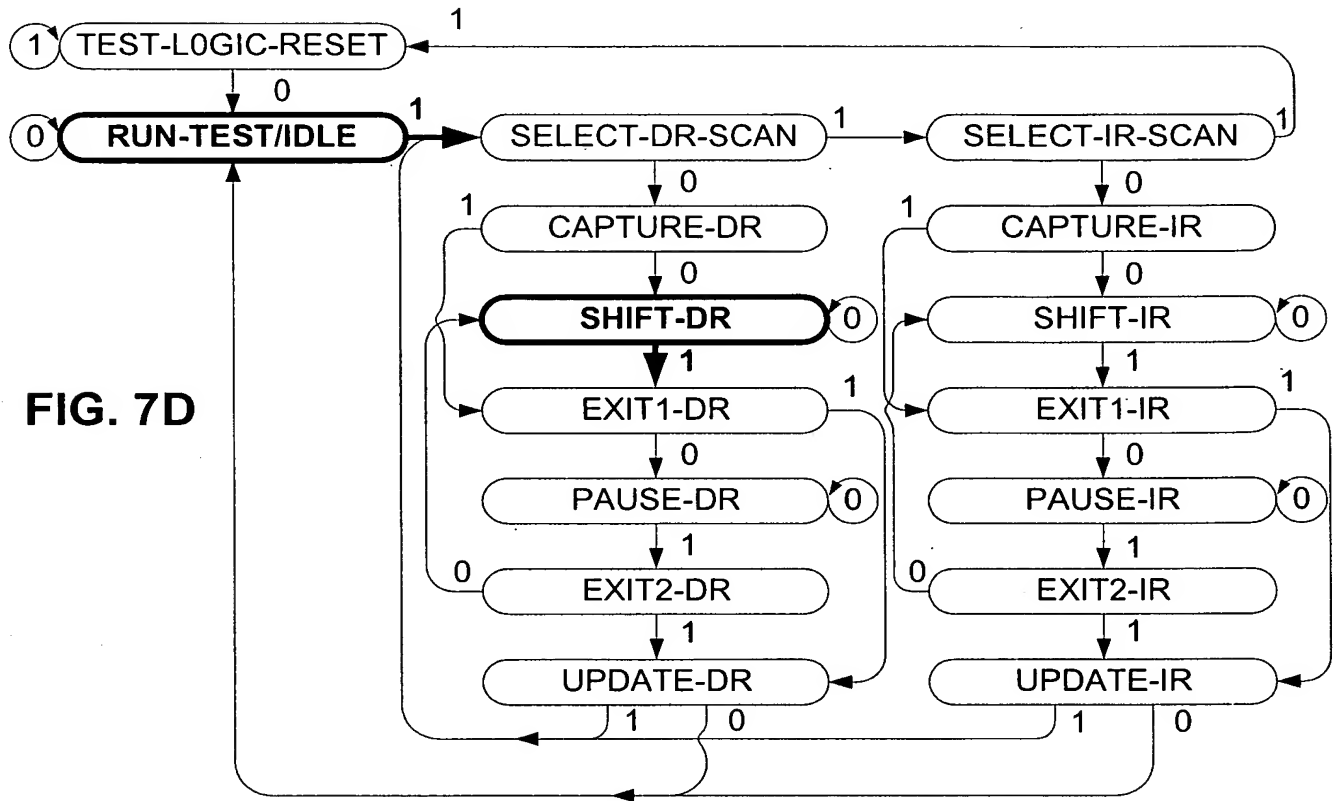


FIG. 7E

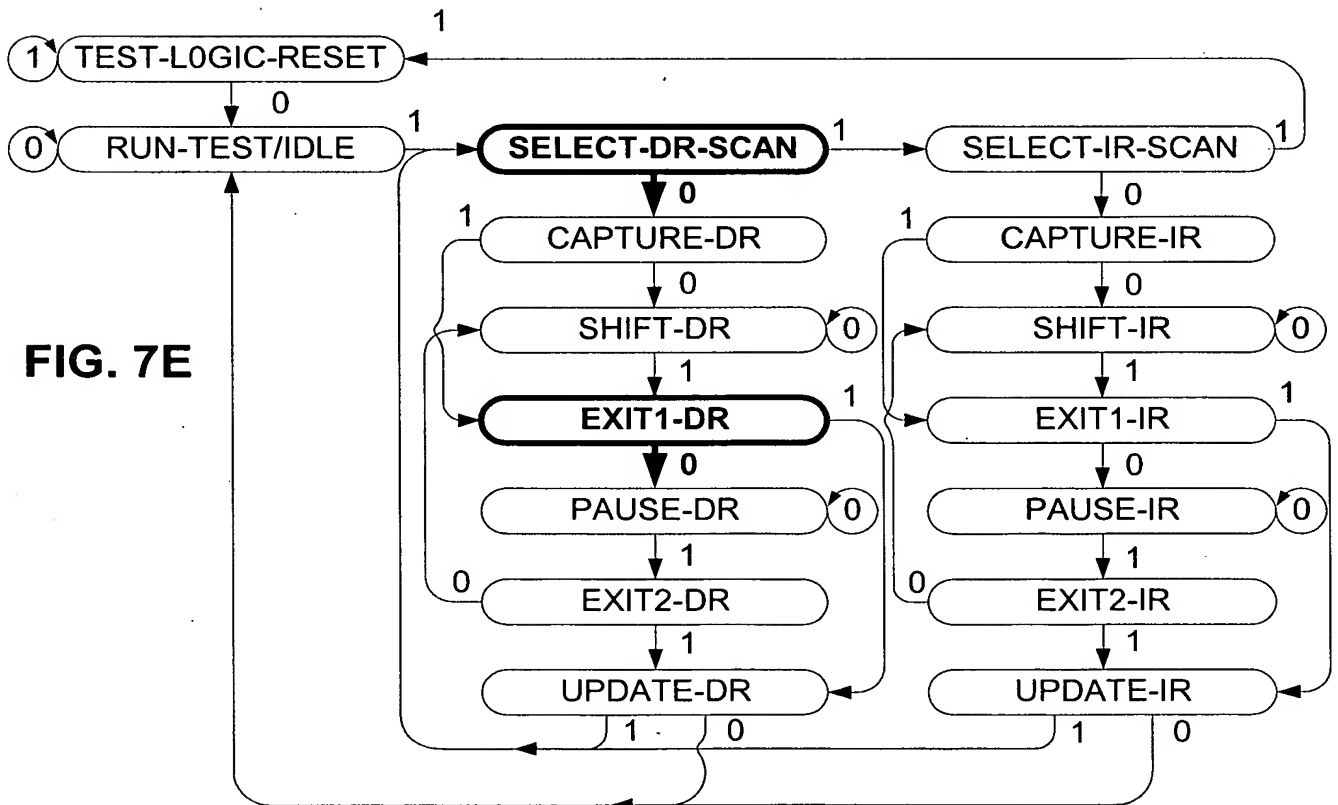




FIG. 7F

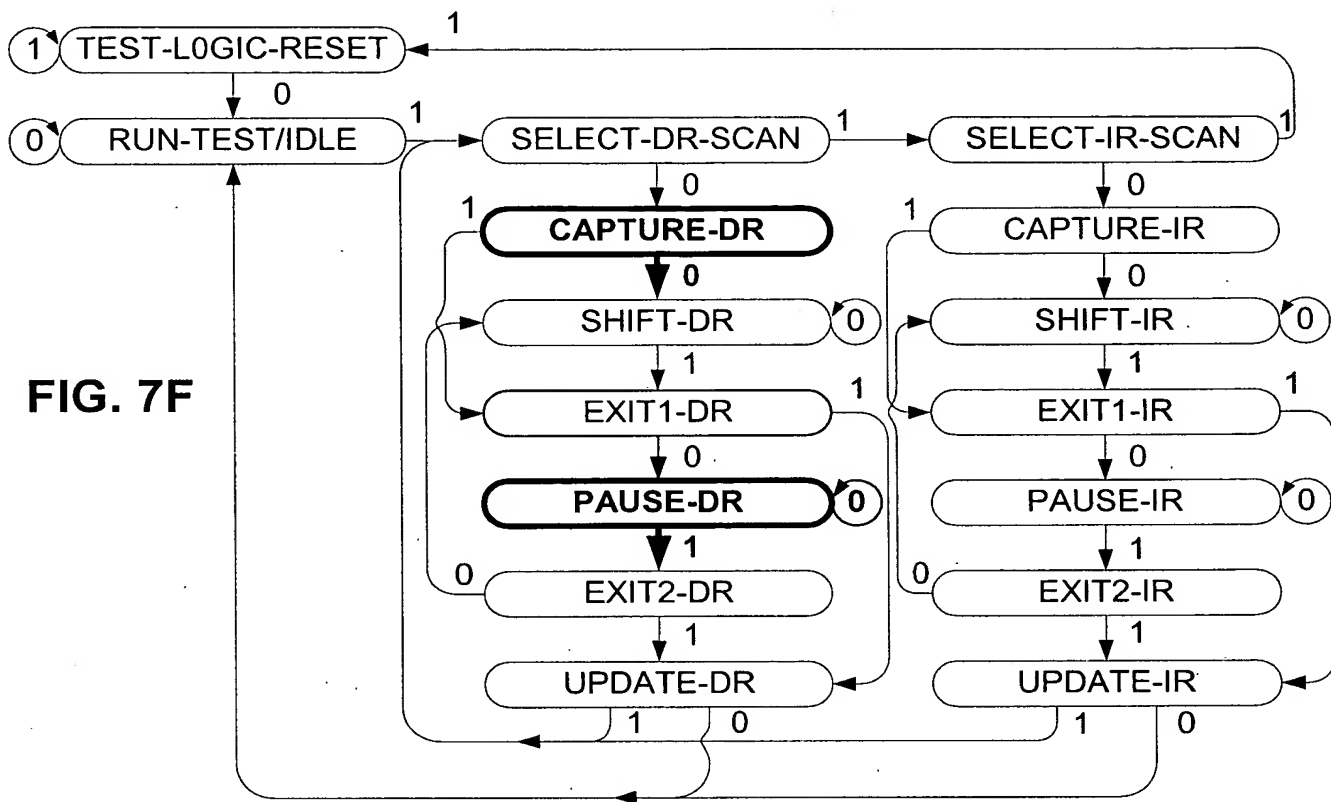
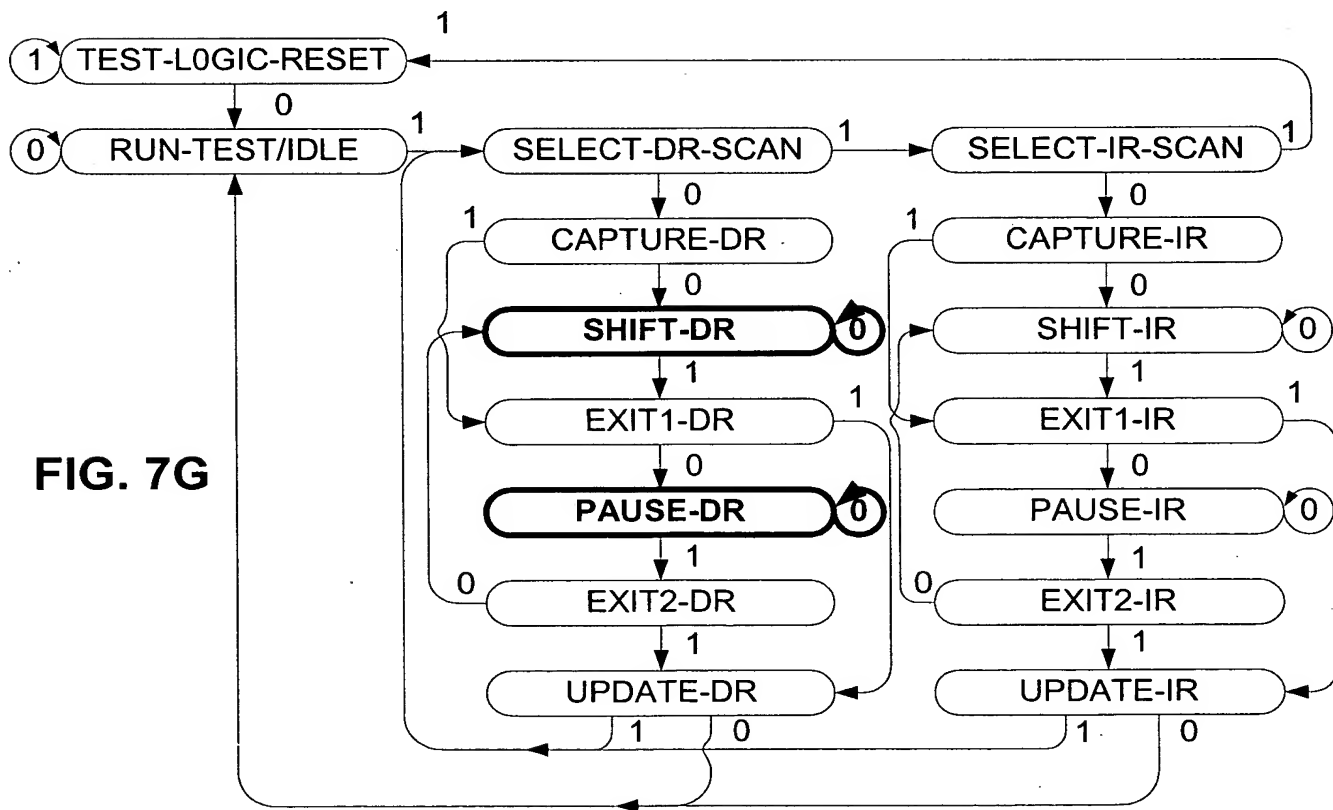


FIG. 7G



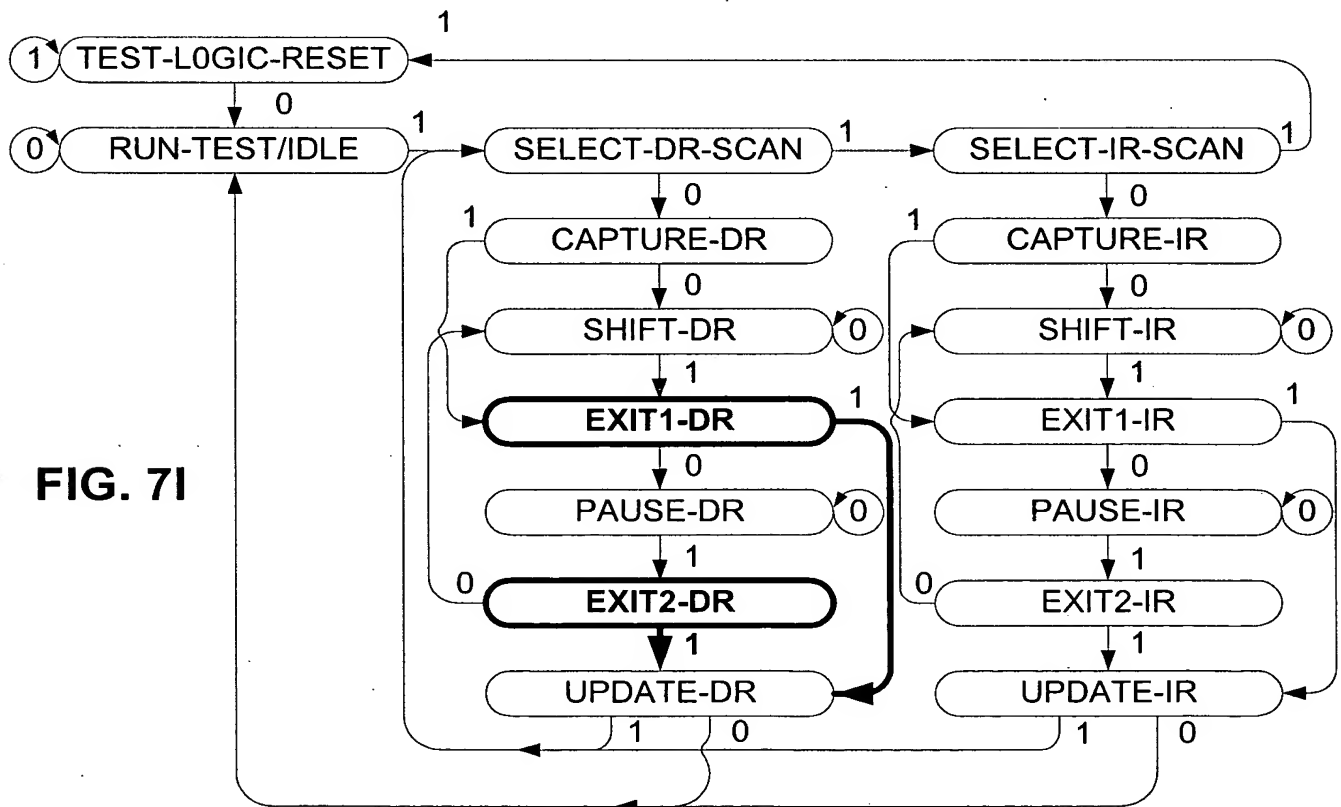
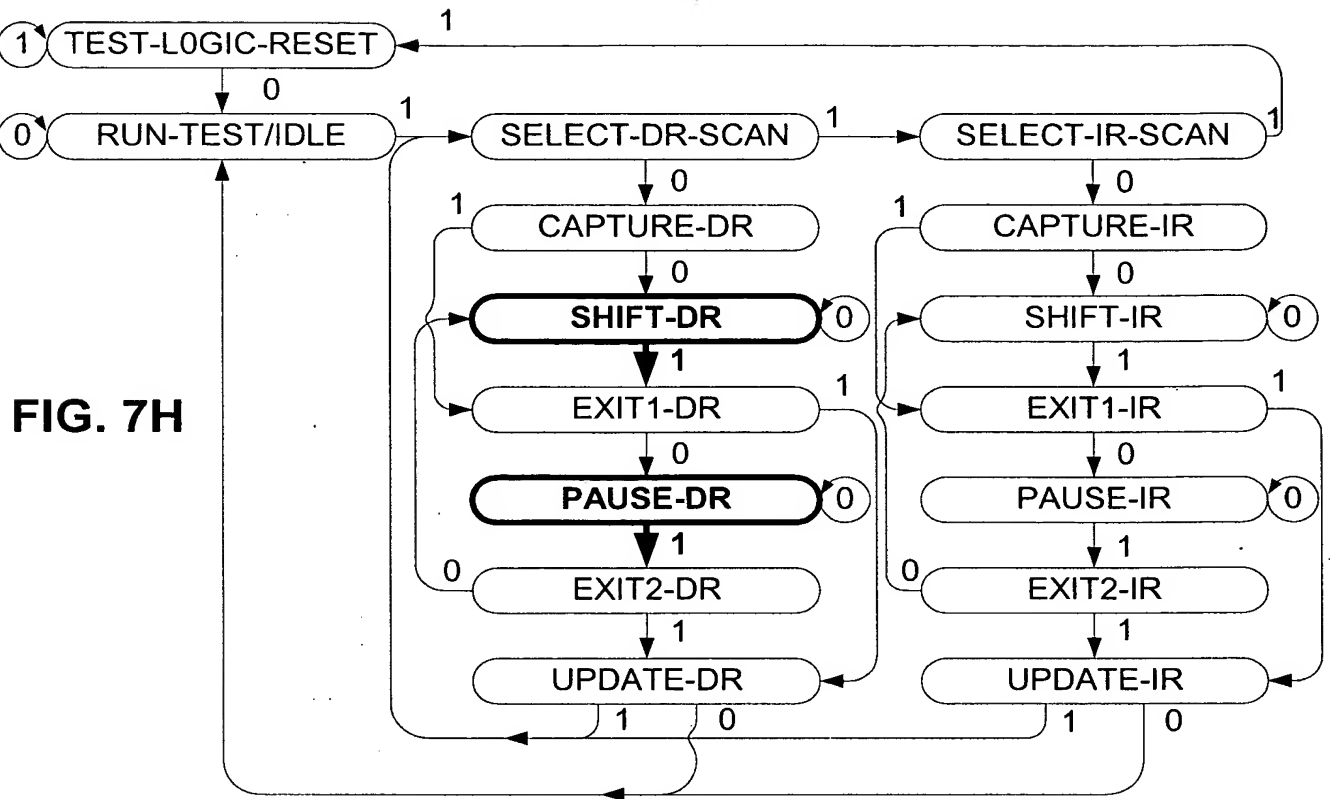


FIG. 7J

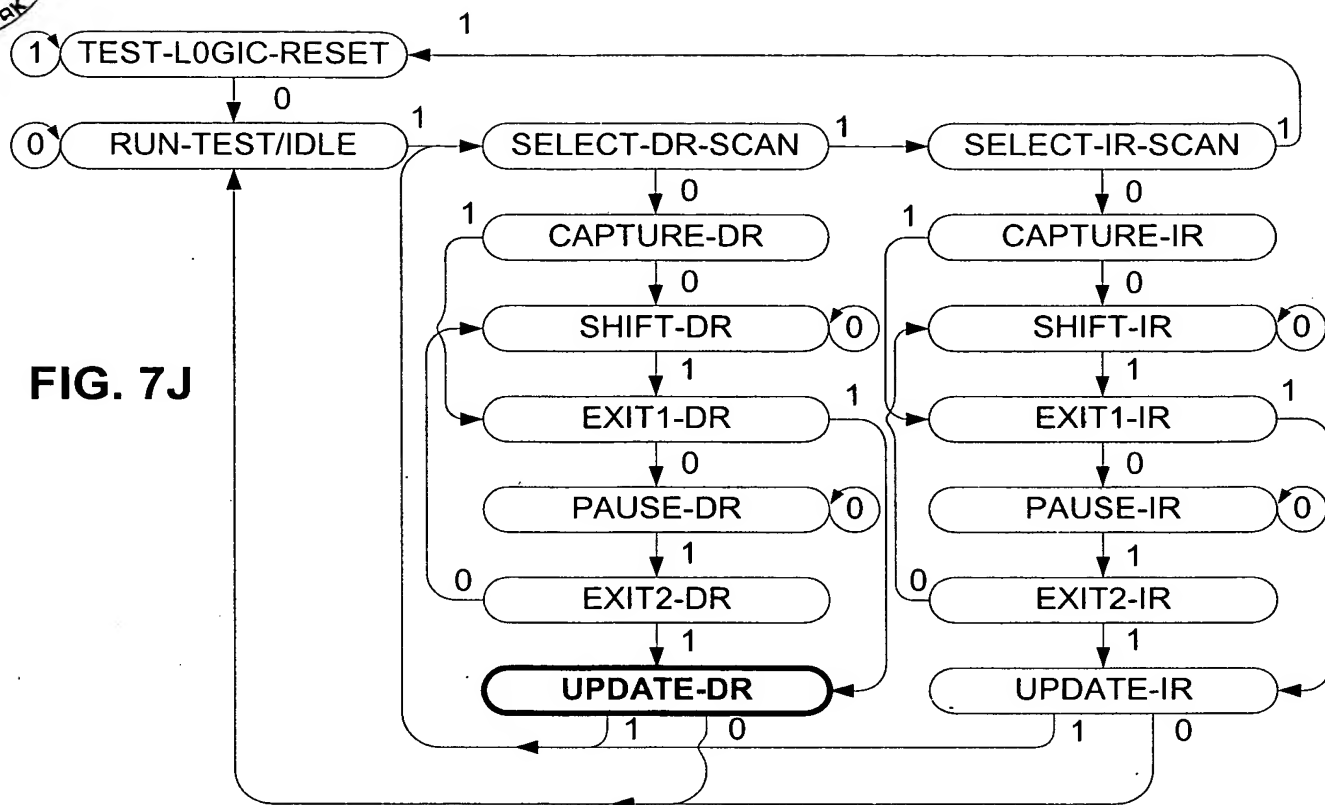


FIG. 8

